

**WHAT IS CLAIMED IS:**

1. A semiconductor device comprising:
  - a plurality of data lines;
  - a plurality of word lines crossing said data lines;
  - dummy word lines crossing said data lines;
  - a memory cell array including a plurality of memory cells arranged at cross-points of said plurality of word lines and data lines;
  - dummy cells arranged at cross-points of said dummy word lines and said data lines; and
  - a sense amplifier coupled to said data lines;

wherein said memory cell array is arranged between said dummy cells and said sense amplifier,

wherein each of the plurality of memory cells includes a read MOS transistor and a write MOS transistor,

wherein each of said dummy cells includes a first dummy read MOS transistor and a first dummy write MOS transistor,

wherein a current flowing through a channel region of the write MOS transistor flows in a direction that crosses a surface of the semiconductor substrate,

wherein a current flowing through a channel region of the first dummy write MOS transistor flows in a direction that crosses the surface of the semiconductor substrate.
2. A semiconductor device according to claim 1,
  - wherein said data line includes a read data line and a write data line, and said dummy cell is arranged for every said read data line.

3. A semiconductor device according to claim 1,  
wherein a resistance value in a source-drain path of the first dummy read MOS transistor is substantially twice of a resistance value of a source-drain path of the read MOS transistor.
4. A semiconductor device according to claim 3,  
wherein the write MOS transistor is formed above the read MOS transistor, and the first dummy write MOS transistor is formed above the first dummy read MOS transistor.
5. A semiconductor device according to claim 1,  
wherein each of said dummy cells further includes a second dummy read MOS transistor coupled to the first dummy read MOS transistor in series.
6. A semiconductor device according to claim 5,  
wherein each of said dummy cells further includes a second dummy write MOS transistor,  
wherein the first dummy write MOS transistor is formed above the first dummy read MOS transistor and the second dummy write MOS transistor is formed above the second dummy read MOS transistor.
7. A semiconductor device according to claim 1,  
wherein the channel region of the write MOS transistor is made of poly crystalline silicon, and  
wherein the channel region of the dummy write MOS transistor is made of poly crystalline.

8. A semiconductor device according to claim 1,  
wherein the direction of the current flowing through the channel region of the write MOS transistor is substantially vertical to the surface of the semiconductor substrate,  
wherein the direction of the current flowing through the channel region of the first dummy write MOS transistor is substantially vertical to the surface of the semiconductor substrate.
9. A semiconductor device according to claim 1,  
wherein each of the plurality of memory cells requires a refreshing operation.